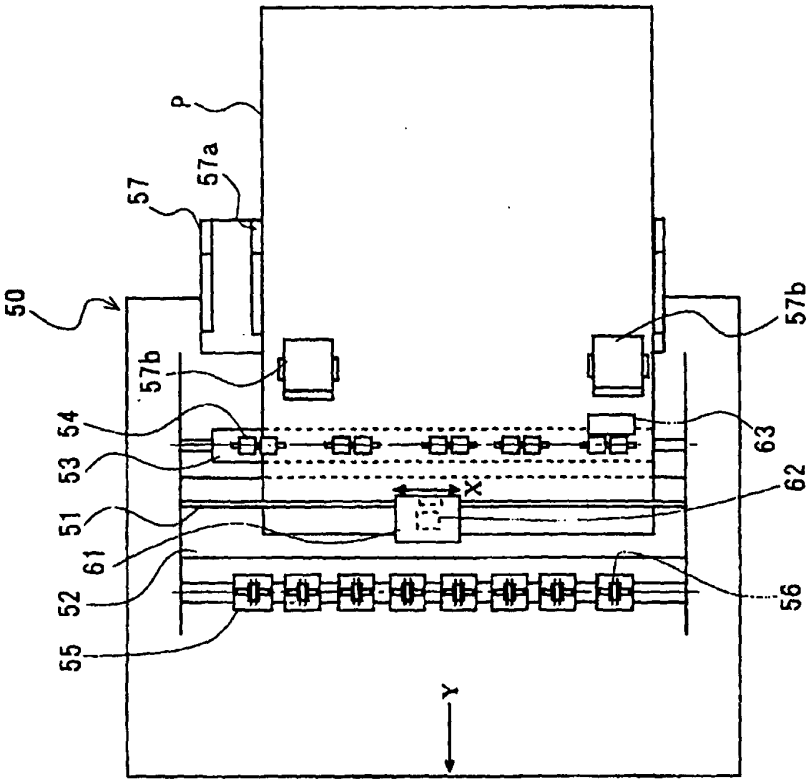
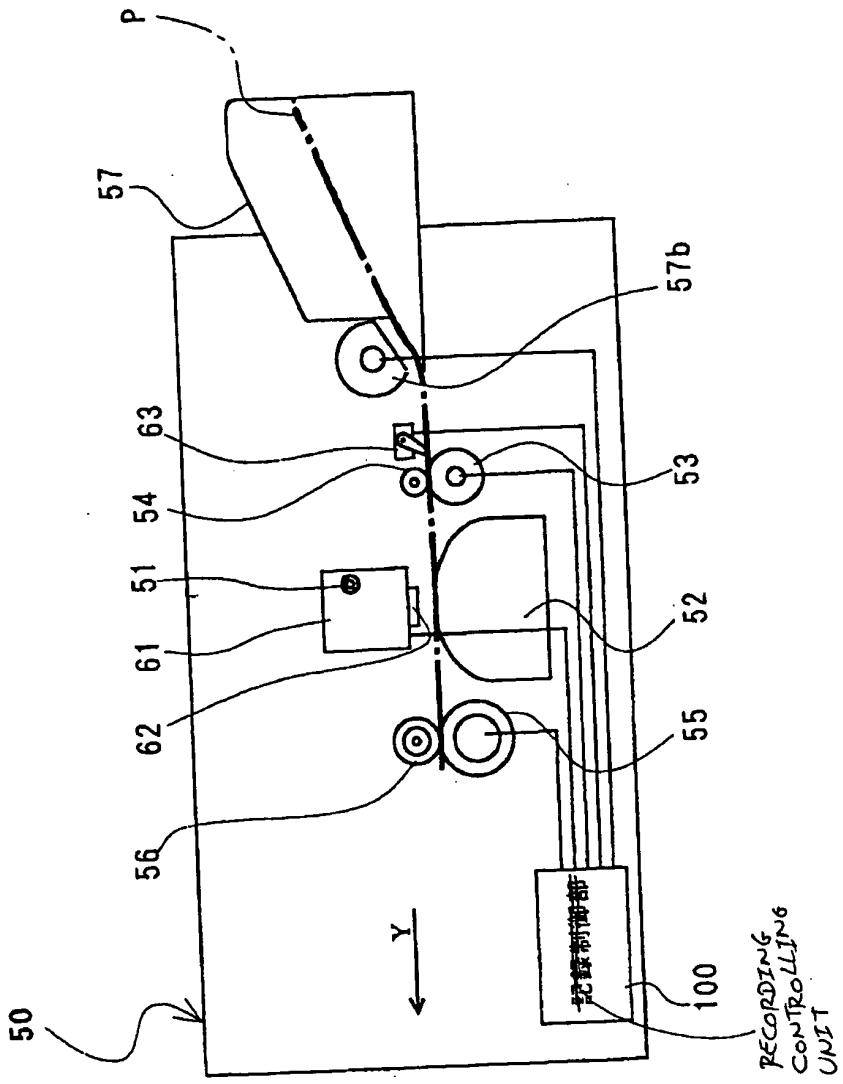
SE-0239 US

【書類名】 ~~図面~~

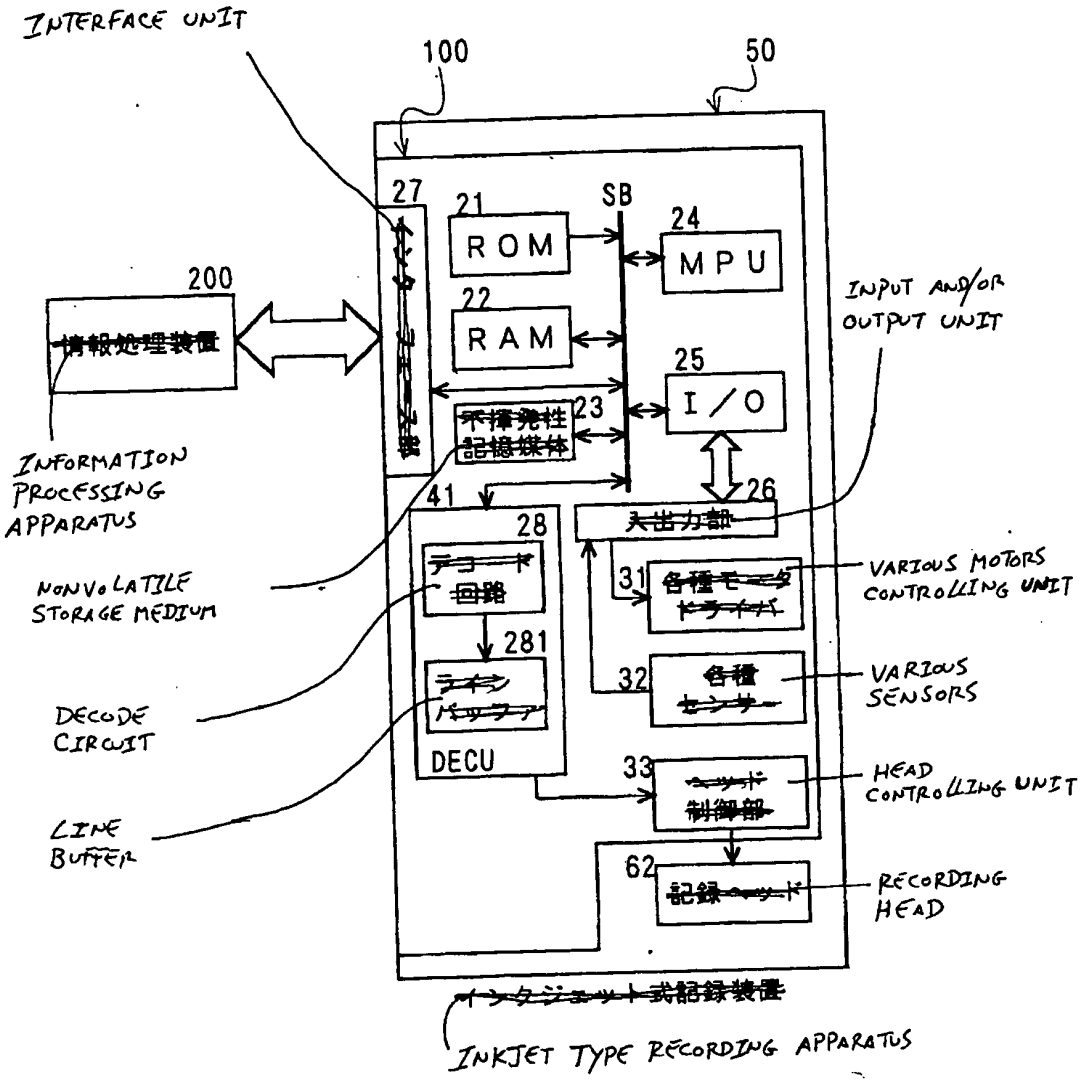
【~~図1~~】 FIG. 1



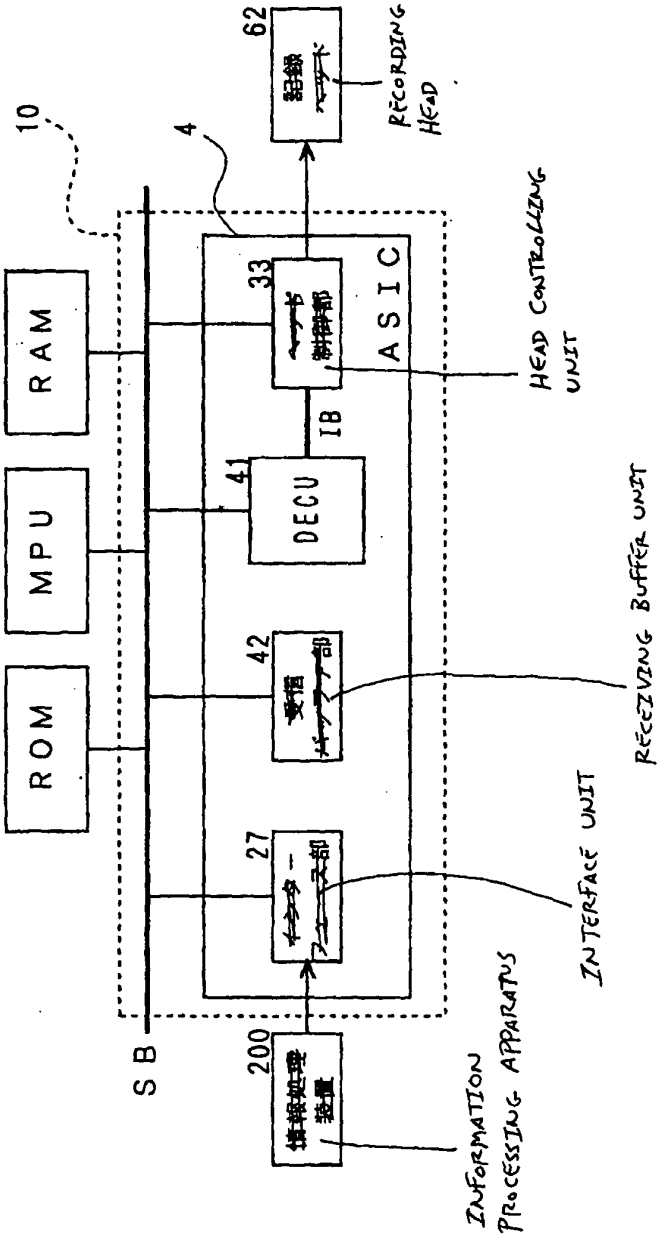
【~~図2~~】
FIG. 2


P
57
57b
63
53
54
51
52
61
62
55
56
Y
記録制御部
50
100
RECORDING CONTROLLING UNIT

【図3】
FIG.3

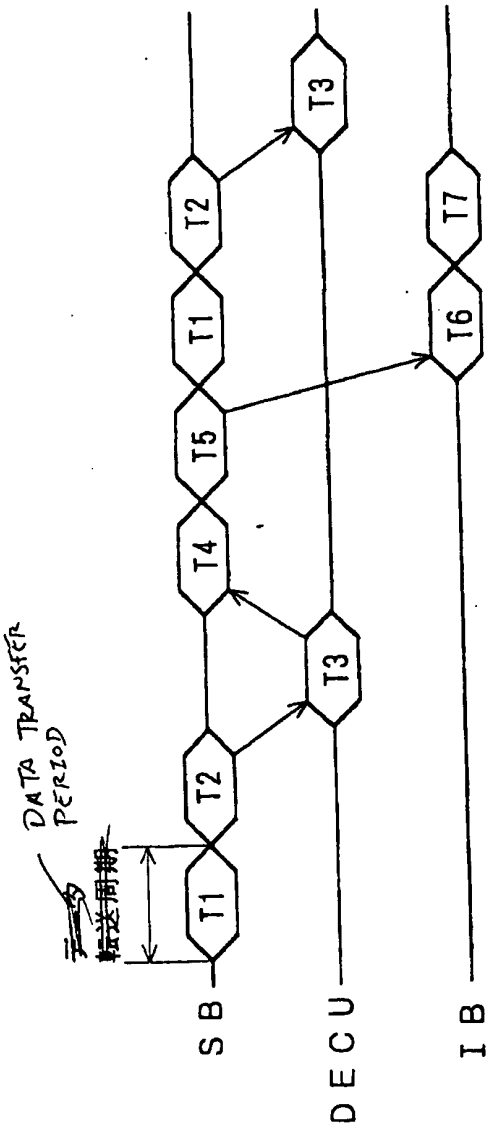

INTERFACE UNIT
100
50
27
21
ROM
SB
24
MPU
200
22
RAM
INPUT AND/OR OUTPUT UNIT
25
I/O
23
26
INFORMATION PROCESSING APPARATUS
41
28
NONVOLATILE STORAGE MEDIUM
31
VARIOUS MOTORS CONTROLLING UNIT
281
32
VARIOUS SENSORS
DECODE CIRCUIT
DECU
33
HEAD CONTROLLING UNIT
LINE BUFFER
62
RECORDING HEAD
INKJET TYPE RECORDING APPARATUS

【図4】
FIG. 4


10
4
62
記録ヘッド
RECORDING HEAD
22
RAM
33
ヘッド制御部
ASIC
HEAD CONTROLLING UNIT
IB
24
MPU
41
DECU
21
ROM
42
受信バッファー部
RECEIVING BUFFER UNIT
27
インターフェース部
INTERFACE UNIT
SB
200
情報処理装置
INFORMATION PROCESSING APPARATUS

【図5】

FIG.5



【図6】

FIG. 6

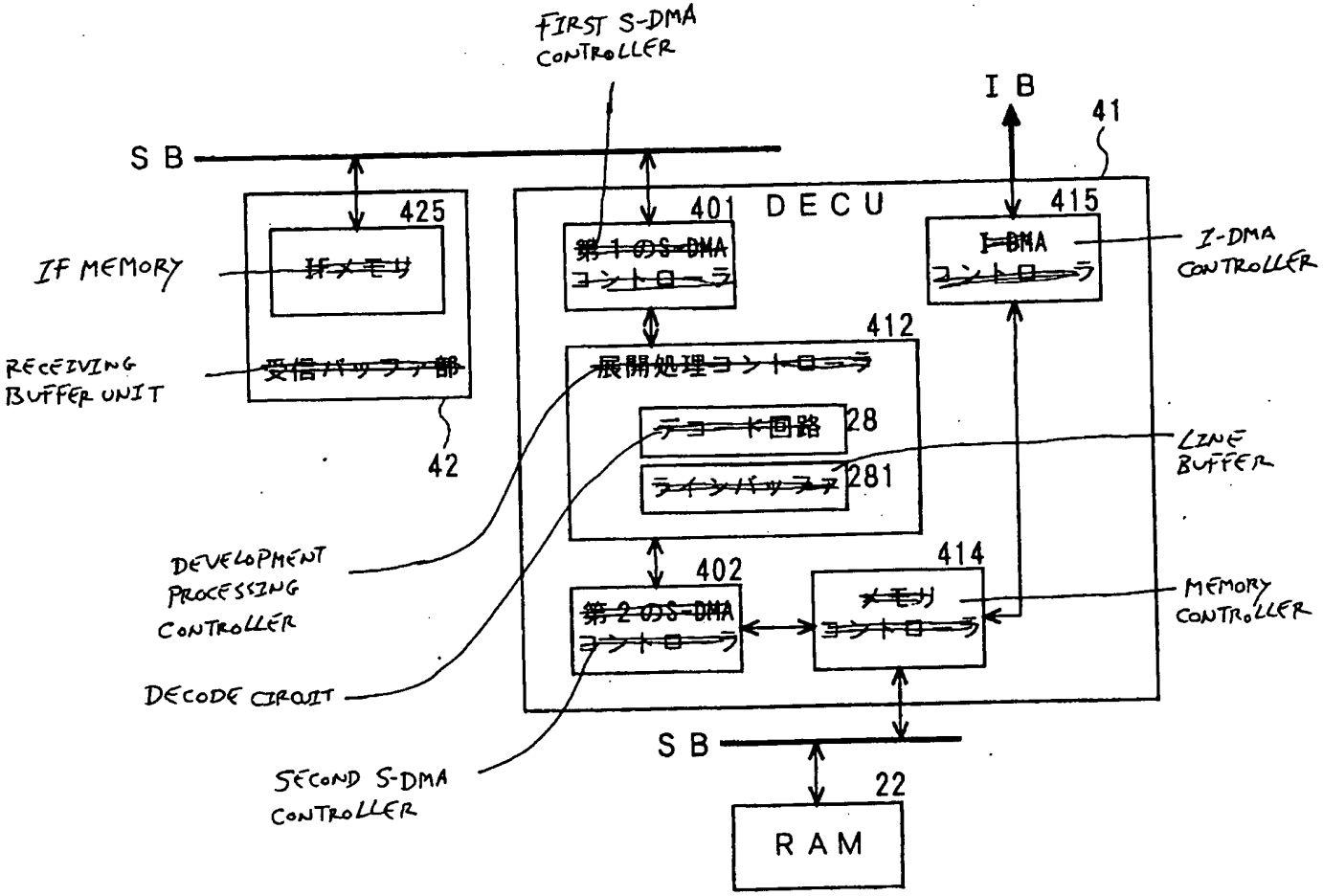
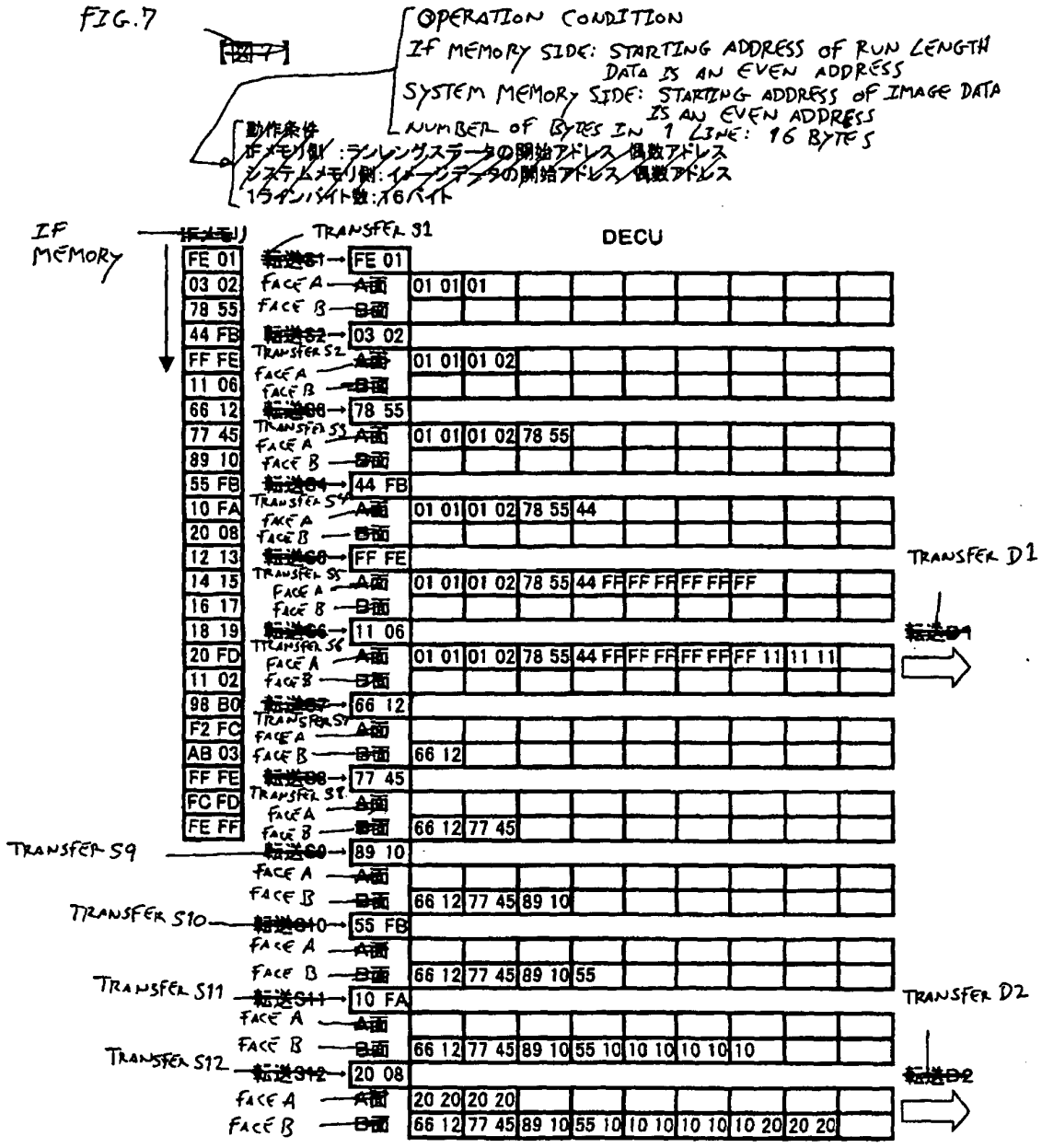
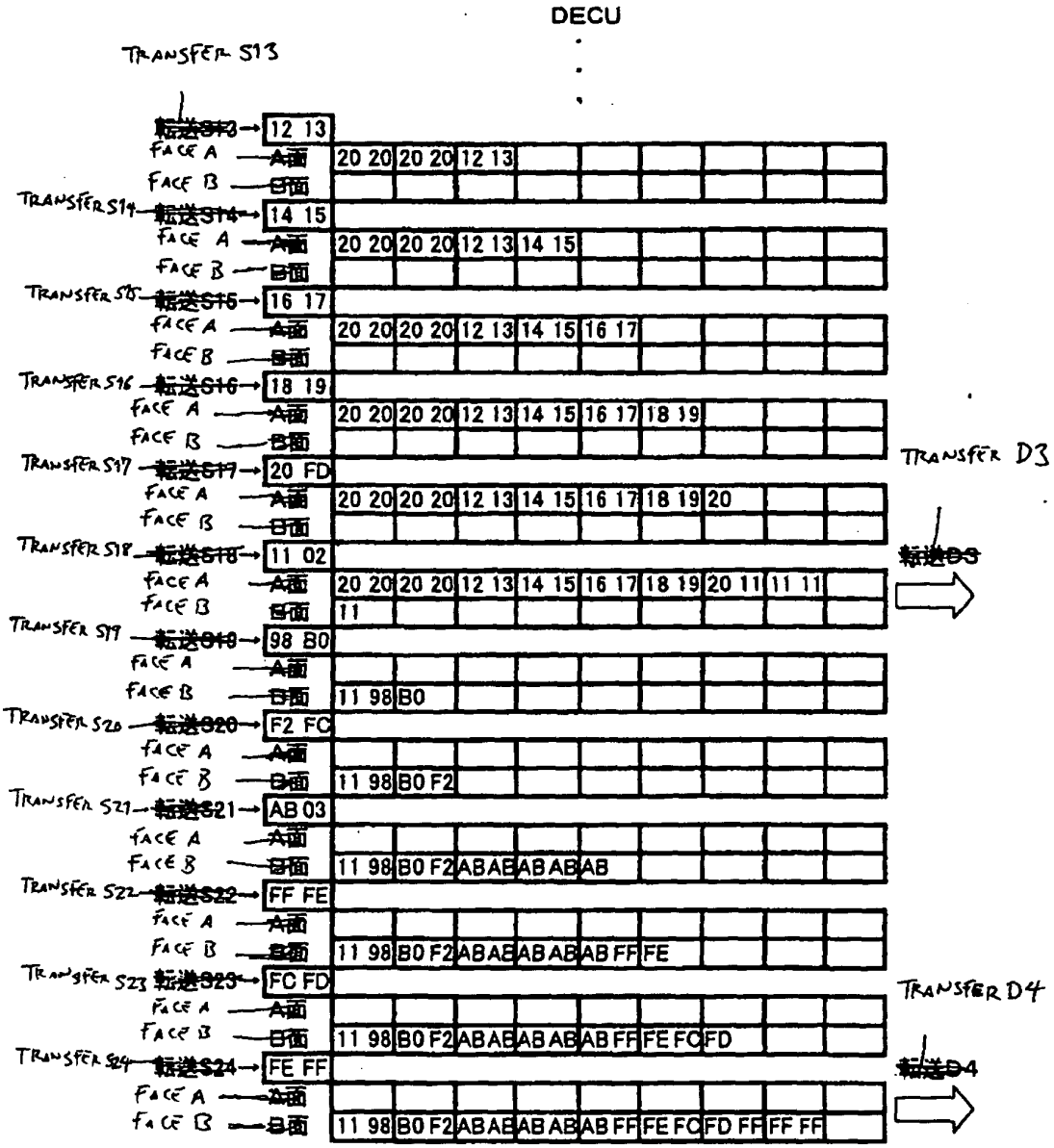

FIRST S-DMA CONTROLLER
I B
41
S B
425
401
DECU
415
IF MEMORY
第1のS-DMA コントローラ
I-DMA コントローラ
I-DMA CONTROLLER
412
RECEIVING BUFFER UNIT
受信バッファ部
展開処理コントローラ
デコード回路
28
LINE BUFFER
ラインバッファ
281
42
DEVELOPMENT PROCESSING CONTROLLER
402
414
第2のS-DMA コントローラ
メモリ コントローラ
MEMORY CONTROLLER
DECODE CIRCUIT
S B
SECOND S-DMA CONTROLLER
22
RAM

FIG.7


OPERATION CONDITION
IF MEMORY SIDE: STARTING ADDRESS OF RUN LENGTH DATA IS AN EVEN ADDRESS
SYSTEM MEMORY SIDE: STARTING ADDRESS OF IMAGE DATA IS AN EVEN ADDRESS
NUMBER OF BYTES IN 1 LINE: 16 BYTES
動作条件
IFメモリ側:ランレングスデータの開始アドレス 偶数アドレス
システムメモリ側:イメージデータの開始アドレス 偶数アドレス
1ラインバイト数:16バイト
IF MEMORY
TRANSFER S1
DECU
FE 01
03 02
78 55
44 FB
FF FE
11 06
66 12
77 45
89 10
55 FB
10 FA
20 08
12 13
14 15
16 17
18 19
20 FD
11 02
98 B0
F2 FC
AB 03
FF FE
FC FD
FE FF
FACE A
FACE B
TRANSFER S2
TRANSFER S3
TRANSFER S4
TRANSFER S5
TRANSFER S6
TRANSFER S7
TRANSFER S8
TRANSFER S9
TRANSFER S10
TRANSFER S11
TRANSFER S12
TRANSFER D1
TRANSFER D2
01 01 01
01 01 01 02
01 01 01 02 78 55
01 01 01 02 78 55 44
01 01 01 02 78 55 44 FF FF FF FF FF
01 01 01 02 78 55 44 FF FF FF FF FF 11 11 11
66 12
66 12 77 45
66 12 77 45 89 10
66 12 77 45 89 10 55
66 12 77 45 89 10 55 10 10 10 10 10
20 20 20 20
66 12 77 45 89 10 55 10 10 10 10 10 20 20 20

~~[図8]~~ FIG. 8


DECU
TRANSFER S13
~~転送S13~~
12 13
FACE A
~~A面~~
20 20 20 20 12 13
FACE B
~~B面~~
TRANSFER S14
~~転送S14~~
14 15
20 20 20 20 12 13 14 15
TRANSFER S15
~~転送S15~~
16 17
20 20 20 20 12 13 14 15 16 17
TRANSFER S16
~~転送S16~~
18 19
20 20 20 20 12 13 14 15 16 17 18 19
TRANSFER S17
~~転送S17~~
20 FD
20 20 20 20 12 13 14 15 16 17 18 19 20
TRANSFER S18
~~転送S18~~
11 02
20 20 20 20 12 13 14 15 16 17 18 19 20 11 11 11
11
TRANSFER S19
~~転送S19~~
98 B0
11 98 B0
TRANSFER S20
~~転送S20~~
F2 FC
11 98 B0 F2
TRANSFER S21
~~転送S21~~
AB 03
11 98 B0 F2 AB AB AB AB AB
TRANSFER S22
~~転送S22~~
FF FE
11 98 B0 F2 AB AB AB AB AB FF FE
TRANSFER S23
~~転送S23~~
FC FD
11 98 B0 F2 AB AB AB AB AB FF FE FC FD
TRANSFER S24
~~転送S24~~
FE FF
11 98 B0 F2 AB AB AB AB AB FF FE FC FD FF FF FF
TRANSFER D3
~~転送D3~~
TRANSFER D4
~~転送D4~~

【図9】

SETTING CONDITION
NO VERTICAL LINE REARRANGEMENT
TOTAL NUMBER OF DEVELOPED BYTES: 64 BYTES (16×4)
NUMBER OF BYTES IN 1 LINE: 16 BYTES
NUMBER OF DEVELOPED LINES: 4 LINES

設定条件
ライン並び変換なし
総展開バイト数:64バイト(16×4)
1ラインバイト数:16バイト
展開ライン数:4ライン

SYSTEM MEMORY

FIG.9A

D1→

01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00

FIG.9B

D2→

01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
66 12	77 45	89 10	55 10
10 10	10 10	10 20	20 20
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00

FIG.9C

D3→

01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
66 12	77 45	89 10	55 10
10 10	10 10	10 20	20 20
20 20	20 20	12 13	14 15
16 17	18 19	20 11	11 11
00 00	00 00	00 00	00 00
00 00	00 00	00 00	00 00

FIG.9D

D4→

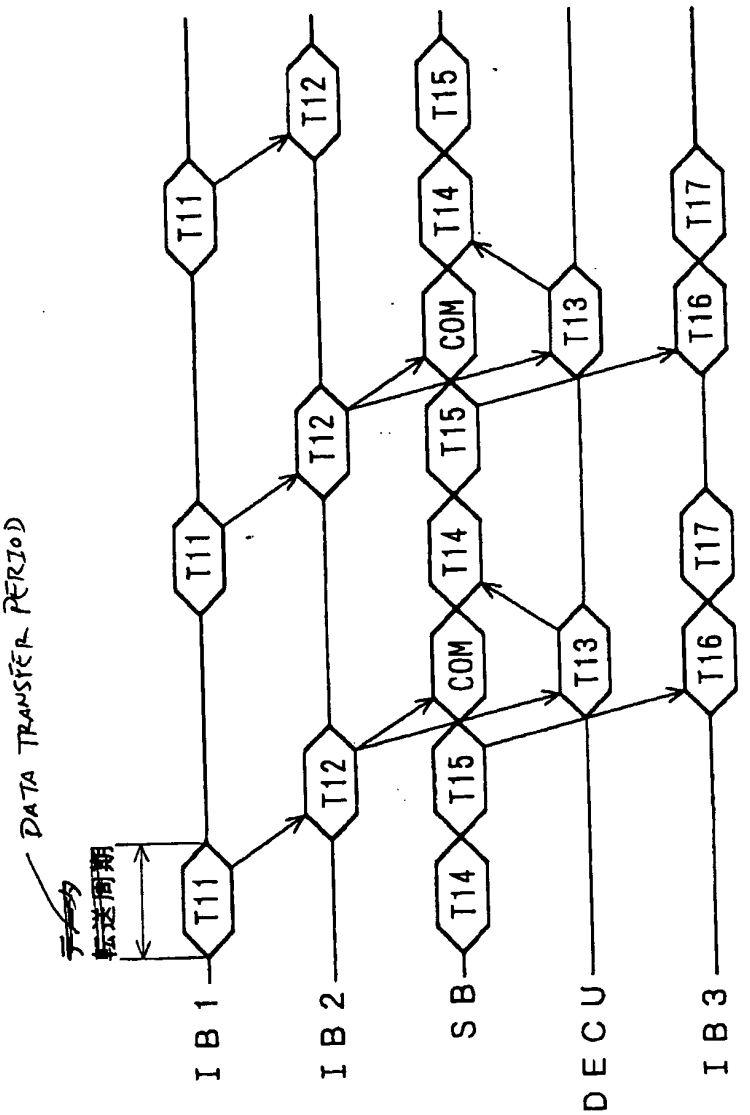
01 01	01 02	78 55	44 FF
FF FF	FF FF	FF 11	11 11
66 12	77 45	89 10	55 10
10 10	10 10	10 20	20 20
20 20	20 20	12 13	14 15
16 17	18 19	20 11	11 11
11 98	B0 F2	ABAB	ABAB
AB FF	FE FC	FD FF	FF FF

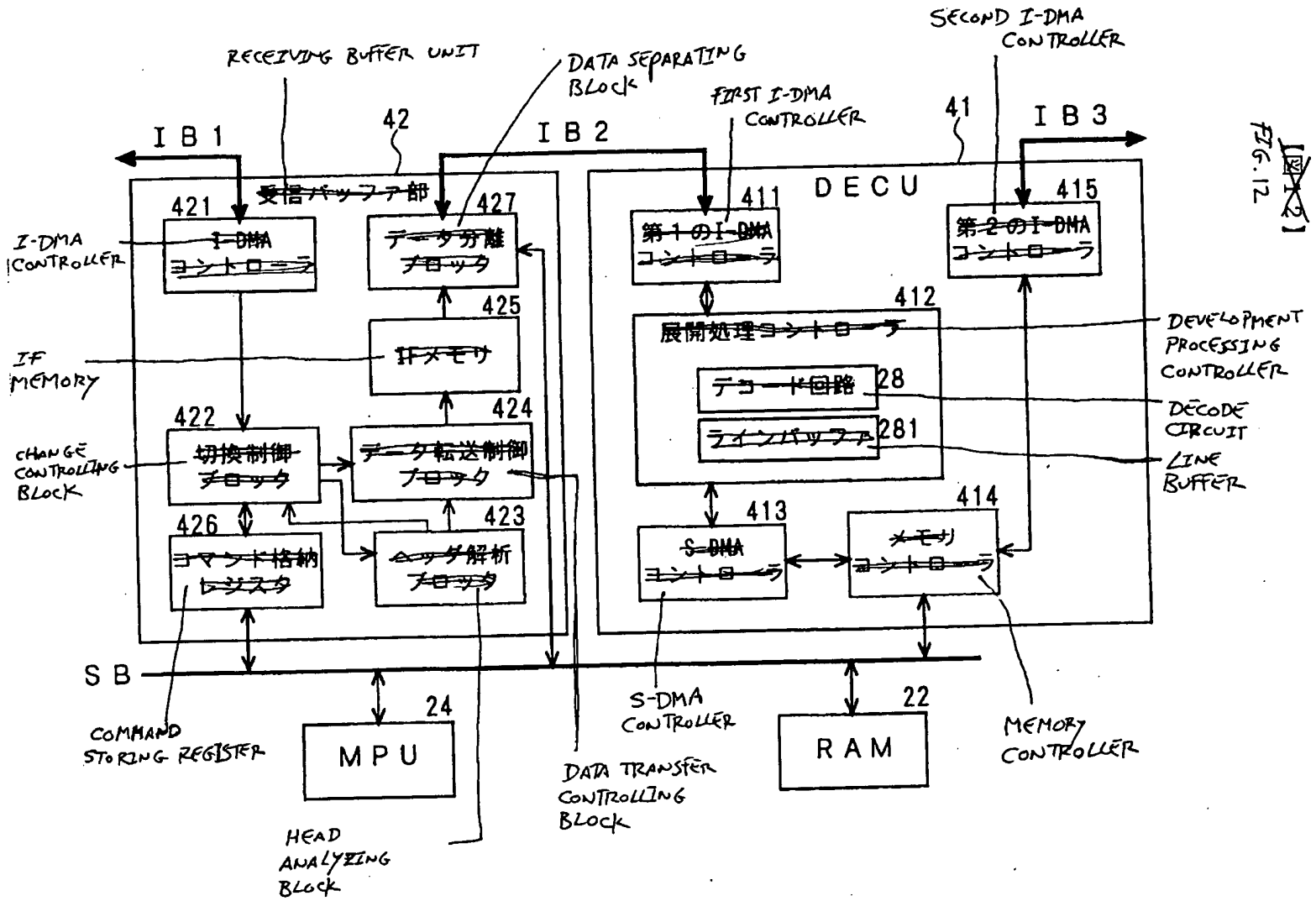
【図10】

FIG.10

10
4
62
RECORDING HEAD
22
RAM
33
ASIC
HEAD CONTROLLING UNIT
24
MPU
41
DECU
IB3
IB2
21
ROM
42
RECEIVING BUFFER UNIT
IB1
27
INTERFACE UNIT
SB
200
INFORMATION PROCESSING APPARATUS

図11
FIG. 11

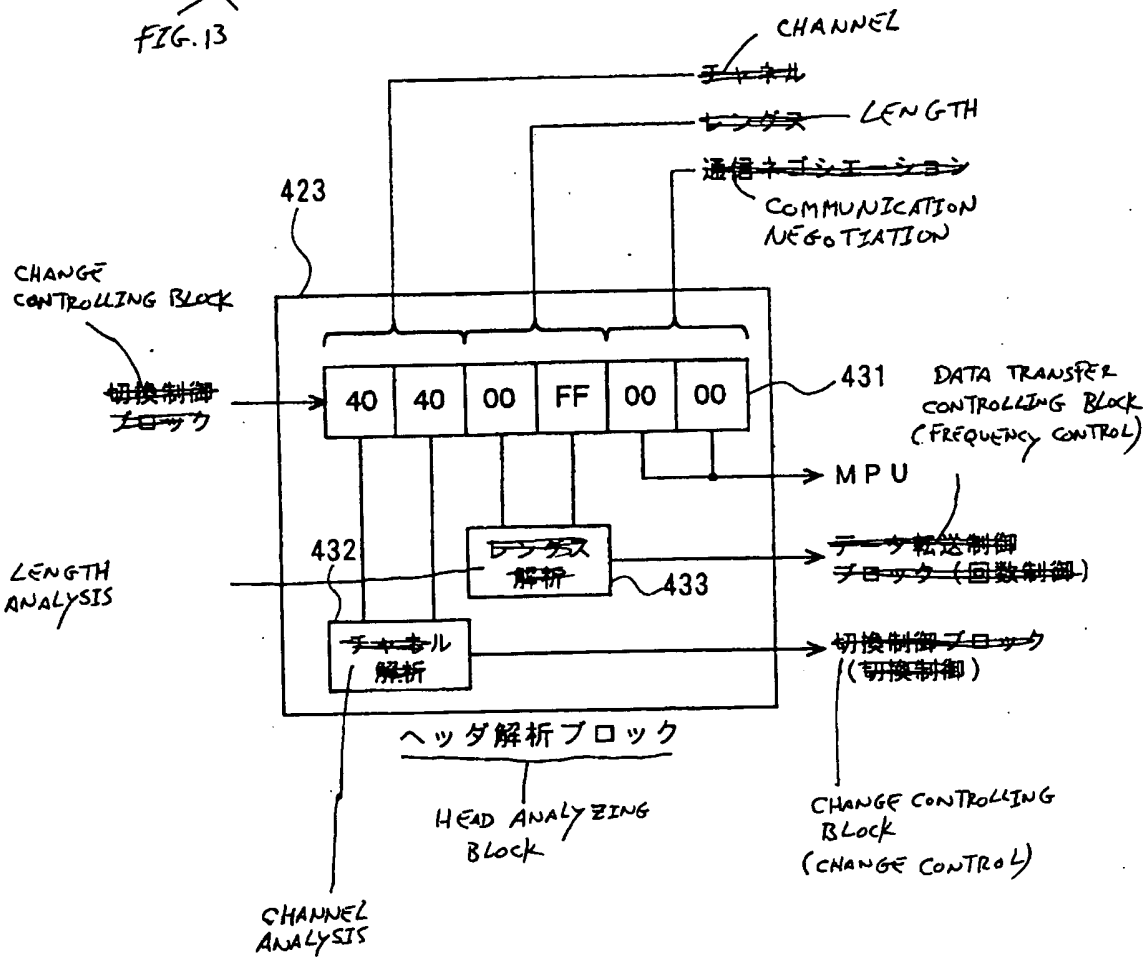

DATA TRANSFER PERIOD
データ転送周期
IB1
IB2
SB
DECU
IB3
T11
T12
T13
T14
T15
T16
T17
COM


RECEIVING BUFFER UNIT
DATA SEPARATING BLOCK
SECOND I-DMA CONTROLLER
FIRST I-DMA CONTROLLER
I B 1
42
I B 2
41
I B 3
DECU
421
427
411
415
I-DMA CONTROLLER
425
412
DEVELOPMENT PROCESSING CONTROLLER
IF MEMORY
28
DECODE CIRCUIT
422
424
281
CHANGE CONTROLLING BLOCK
LINE BUFFER
426
423
413
414
S B
24
22
COMMAND STORING REGISTER
MPU
S-DMA CONTROLLER
RAM
MEMORY CONTROLLER
DATA TRANSFER CONTROLLING BLOCK
HEAD ANALYZING BLOCK

【図12】
FIG. 12

【図13】

FIG. 13


CHANNEL
LENGTH
COMMUNICATION NEGOTIATION
423
CHANGE CONTROLLING BLOCK
40
40
00
FF
00
00
431
DATA TRANSFER CONTROLLING BLOCK (FREQUENCY CONTROL)
MPU
LENGTH ANALYSIS
432
433
CHANNEL ANALYSIS
ヘッダ解析ブロック
HEAD ANALYZING BLOCK
CHANGE CONTROLLING BLOCK (CHANGE CONTROL)

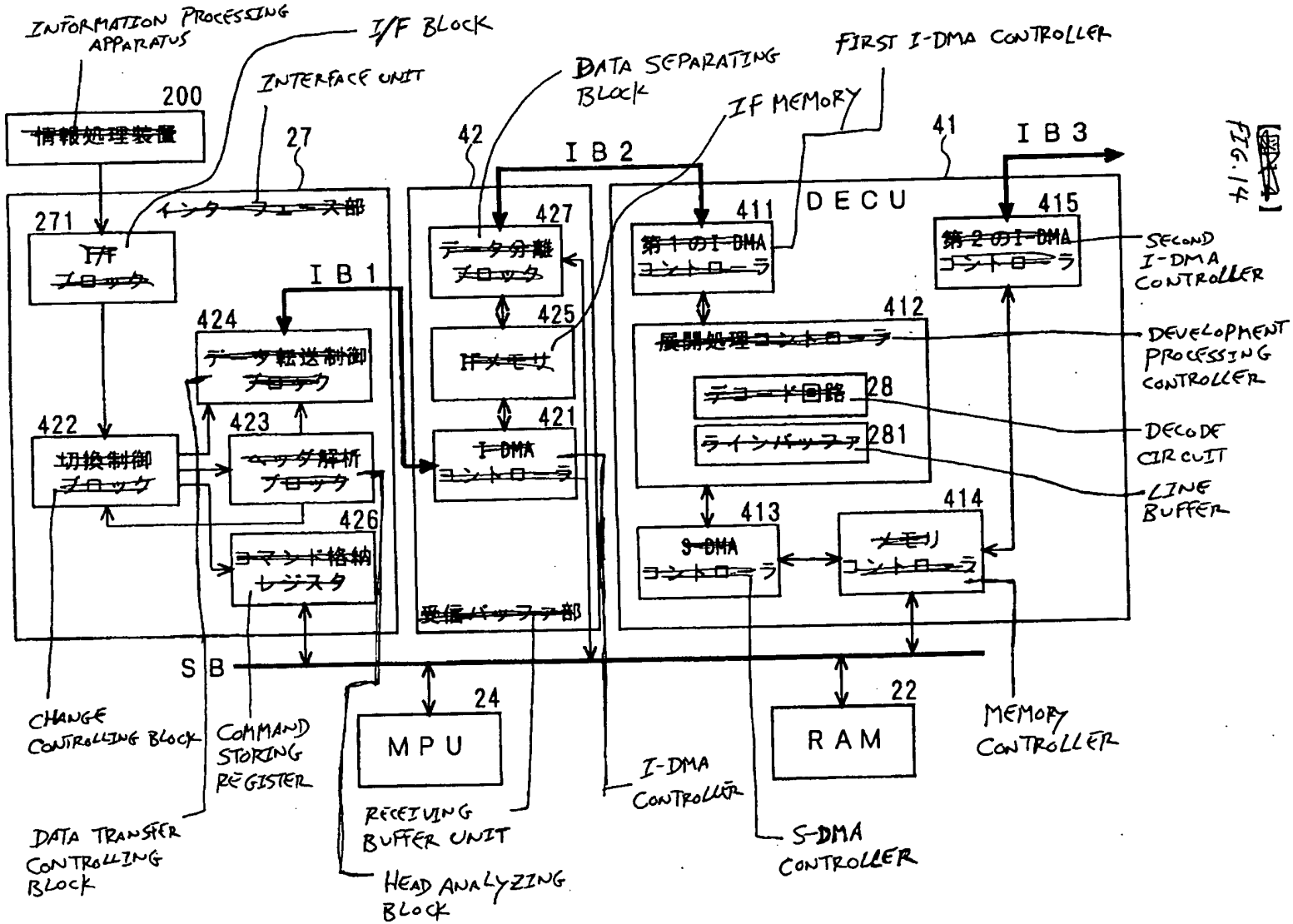
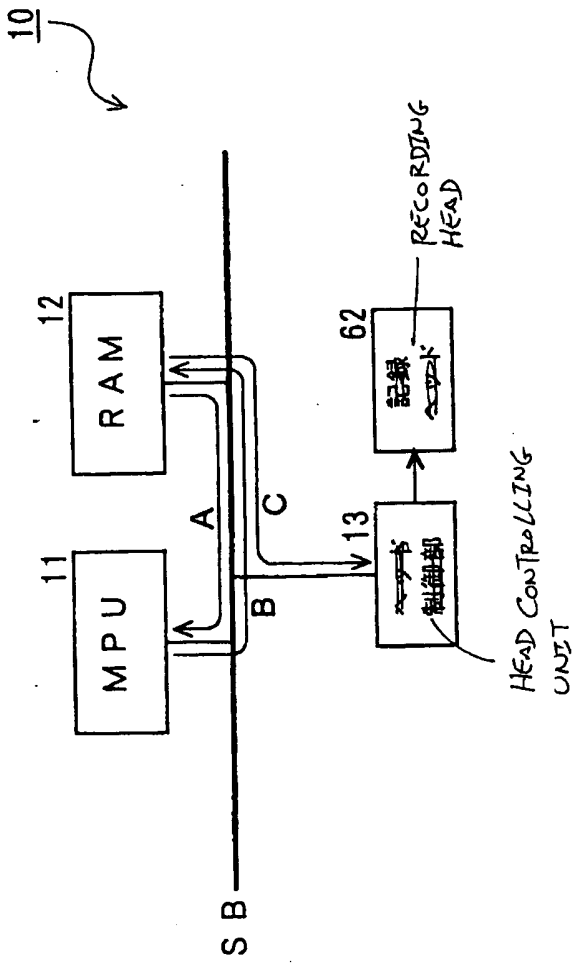

INFORMATION PROCESSING APPARATUS
200
情報処理装置
I/F BLOCK
INTERFACE UNIT
27
インターフェース部
271
I/F ブロック
DATA SEPARATING BLOCK
42
IB2
427
データ分離ブロック
425
IFメモリ
421
I-DMA コントローラ
受信バッファ部
FIRST I-DMA CONTROLLER
IF MEMORY
41
IB3
DECU
411
第1のI-DMA コントローラ
415
第2のI-DMA コントローラ
SECOND I-DMA CONTROLLER
412
展開処理コントローラ
DEVELOPMENT PROCESSING CONTROLLER
デコード回路
28
DECODE CIRCUIT
ラインバッファ
281
LINE BUFFER
IB1
424
データ転送制御ブロック
422
切換制御ブロック
423
ヘッダ解析ブロック
426
コマンド格納レジスタ
413
S-DMA コントローラ
414
メモリコントローラ
MEMORY CONTROLLER
SB
24
MPU
RECEIVING BUFFER UNIT
HEAD ANALYZING BLOCK
22
RAM
I-DMA CONTROLLER
S-DMA CONTROLLER
CHANGE CONTROLLING BLOCK
COMMAND STORING REGISTER
DATA TRANSFER CONTROLLING BLOCK

FIG. 14 【図14】

【図15】

FIG.15


10
12
RAM
11
MPU
A
B
C
13
62
RECORDING HEAD
HEAD CONTROLLING UNIT
SB